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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HYUN, SOON D	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,664	HUNG ET AL.	
	Examiner	Art Unit	
	Soon D. Hyun	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4-7,9,10,20,21 and 23-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-32* is/are allowed.

6)☒ Claim(s) *2,4-6,9,10,20,21 and 25-27* is/are rejected.

7)☒ Claim(s) *7,23,24 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

ANDREW C. LEE
PRIMARY PATENT EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 2, 4, 6, 9, 10, 20, 21, and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Akella et al (U.S. Patent No. 6,697,362).

Regarding claims 2 and 20, Akella et al (Akella) discloses a system and method comprising:

a memory (a memory pool 227 in FIG. 3), wherein the memory includes a plurality of logical memory devices (227a-227d in FIG. 3); and

a network switch (switch stage 215 in FIG. 3, a switch engine 230, Table RAM 240, and memory switch 220 in FIG. 3) coupled to the memory, the network switch including a memory controller (switch interface 30 in FIG. 5+ the switch engine 230 in FIG. 3 + memory switch 220 in FIG. 3), wherein the switch sequentially writes a first portion (250a in FIG. 5) of received packet data to a first (227a in FIG. 3) of the logical memory devices and writes a second portion (250b In FIG. 5) of the packet data to a second (227b in FIG. 3) of the logical memory devices and writes a third portion (250c

in FIG. 5) of the packet data to a third (227c in FIG. 3) of the logical memory devices (col. 7, line 55-col. 8, line 15) and

wherein N portions of a packet are stored at addresses 0-N in a memory pool 225 (address N indicates one of the memory devices 227a-227d, because each portion is stored in one of the memory devices) and switch interface 30 will keep track so that an initial portion of a next received packet is stored at address N+1, i.e., N is the address of a memory device that was last written. Therefore, the switch interfacehas a record identifying a memory device that was last written (col. 7, lines 51-52 and col. 8, lines 31-65).

Regarding claim 4, Akella further discloses that the memory controller comprises a first memory controller component (a memory ASIC 252a in FIG. 3) coupled to the first logical memory device (227a) and a second memory controller component (a memory ASIC 252b in FIG. 3) coupled to the second logical memory device (227b).

Regarding claim 6, Akella further teaches that the memory pool (227a-227d) cane formed by a plurality of DRAM type devices (col. 6, lines 35-36), i.e., SDRAM for can be formed for the memory pool, because the SDRAM is a type of DRAM.

Regarding claim 9, Akella further discloses that the network switch further comprises:

a receiver (a port module 210) coupled to the memory controller (the switch engine 230 + Table RAM 240 + memory switch 220);

a transmitter (the port module 210) coupled to the memory controller;

address resolution logic (a switch interface 30 in Fig. 5, col. 7, lines 48-51) coupled to the memory controller; and

packet queuing control (RX 22-1 and TX 24-1 in FIG. 5) coupled to the memory controller, the receiver, the transmitter and the address resolution logic.

Regarding claim 10, Akella teaches that the network switch further comprises a media access controller (MAC) coupled to the receiver (the MAC is not shown, but the MAC is inherently required for each port , because the port receives packets of LAN, col. 4, lines 53-56), wherein the MAC receives packet data via a plurality of ports (210-1 to 210-n) coupled to the receiver.

Regarding claim 21, refer to the discussion for claims 2 and 20. Same procedure for the second packet is performed (see FIG. 6).

Regarding claim 25, refer to the discussion for claim 2, Akella discloses a method of switching packets within a network switch comprising:

receiving a first data packet (S30 in FIG. 6) from a first port (210-1 in FIG. 3);

parsing the first data packet into a plurality of packet portions (S70);

writing a first portion (250a) of the first packet to a first logical memory device (227a) of a plurality of logical memory devices (225);

writing a second portion (250b) of the first data packet to a second logical memory device (227b) of the plurality of logical memory devices;

same procedure as for the first packet is performed for a second packet (see FIG. 6);

determining which of the plurality of logical memory devices was the last of the plurality of memory devices to which one of the plurality of first data packet portions was written (col. 7, lines 31-40); and

writing a first portion of the second data packet to one (227a) of the logical memory devices other than the last (227d) of the plurality of memory devices (col. 7, line 66-col. 8, line 15), e.g., each 64-byte packet (the first packet and the second packet) is parsed into four 16-byte packet portions and the first portion (16-byte) of the second 64-byte packet is stored at memory device 227a (the first logical device of claim 26) and the last portion of the first packet is stored at memory device 227d.

Regarding claim 27, Akella further discloses that the second portion of the second data packet is stored at 227b (other than the last memory device 227d).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akella et al (U.S. Patent No. 6,697,362) in view of Mills et al (U.S. Patent No. 5,684,752).

Akella et al (Akella) does not explicitly teach that the memory controller components access the corresponding logical memory devices via a shared address line. Mills et al (Mills) teach that a shared address line is used to reduce address lines

(col. 1, lines 53-55). Those of skill in the art would have been motivated by Mills to use a shared address line to reduce address lines. Therefore it would have been obvious to one having ordinary skill in the art to incorporate a shared address line into Akella to reduce address lines.

Allowable Subject Matter

5. Claims 29-32 are allowed.

Response to Arguments

6. Applicant's arguments filed 12/22/2005 have been fully considered but they are not persuasive.

Regarding claims 2, 20, and 25, Applicant argues (Remarks page 10, lines 5-7, page, 12, lines 2-4, page 13, lines 8-9) that Akella fail to discloses a memory controller that maintains a record identifying which of the plurality of logical memory devices was last written to. Examiner disagrees. With reference to col. 8, lines 31-65), N portions of a packet are stored at addresses 0-N in a memory pool 225 (address N indicates one of the memory devices 227a-227d, because each portion is stored in one of the memory devices) and switch interface 30 will keep track so that an initial portion of a next received packet is stored at address N+1, i.e., N is the address of a memory device that was last written. Therefore, the switch interface has a record identifying a memory device that was last written.

For the reasons as discussed above, examiner believes that the claim rejection is proper.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Soon D. Hyun whose telephone number is 571-272-3121. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Hyun
09/12/2005

ANDREW C. LEE
PRIMARY PATENT EXAMINER